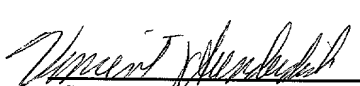




U.S. APPLICATION NO (if known, see 37 CFR 1.53) <b>09/623894</b>		INTERNATIONAL APPLICATION NO PCT/EP99/01165		ATTORNEY'S DOCKET NUMBER 951/49162	
17. <input checked="" type="checkbox"/> The following fees are submitted:				CALCULATIONS	PTO USE ONLY
Basic National Fee (37 CFR 1.492(a)(1)-(5)): Search Report has been prepared by the EPO or JPO ..... \$840.00 International preliminary examination fee paid to USPTO (37 CFR 1.482) ... \$670.00 No international preliminary examination fee paid to USPTO (37 CFR 1.482) but international search fee paid to USPTO (37 CFR 1.445(a)(2)) ..... \$760.00 Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO ..... \$ 970.00 International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(2)-(4) ..... \$96.00				840.00	
ENTER APPROPRIATE BASIC FEE AMOUNT =				\$ 840.00	
Surcharge of \$130.00 for furnishing the oath or declaration later than <input type="checkbox"/> 20 <input type="checkbox"/> 30 months from the earliest claimed priority date (37 CFR 1.492(e)).				\$ 130.00	
Claims	Number Filed	Number Extra	Rate		
Total Claims	4-20=		X \$18.00	\$	
Independent Claims	2-3=		X \$78.00	\$	
Multiple dependent claims(s) (if applicable)			+ \$260.00	\$	
TOTAL OF ABOVE CALCULATIONS =				\$ 130.00	
Reduction by 1/2 for filing by small entity, if applicable. Verified Small Entity statement must also be filed. (Note 37 CFR 1.9, 1.27, 1.28).				\$	
SUBTOTAL =				\$ 970.00	
Processing fee of \$130.00 for furnishing the English translation later than <input type="checkbox"/> 20 <input type="checkbox"/> 30 months from the earliest claimed priority date (37 CFR 1.492(f)).				\$	
TOTAL NATIONAL FEE =				\$ 970.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). \$40.00 per property +				\$	
TOTAL FEE ENCLOSED =				\$ 970.00	
				Amount to be: refunded	\$
				charged	\$
a. <input checked="" type="checkbox"/> A check in the amount of \$ <b>970.00</b> for the filing fee is enclosed b. <input type="checkbox"/> Please charge my Deposit Account No. _____ in the amount of \$ _____ to cover the above fees. A duplicate copy of this sheet is enclosed. c. <input checked="" type="checkbox"/> The Commissioner is hereby authorized to charge any additional fees, which may be required, or credit any overpayment to Deposit Account No. <u>05-1323</u> (Attorney Docket No. <b>951/49162</b> ). A duplicate copy of this sheet is enclosed.					
NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.					
SEND ALL CORRESPONDENCE TO: Evenson, McKeown, Edwards & Lenahan, P.L.L.C. 1200 G Street, N.W., Suite 700 Washington, D.C. 20005 Tel. No. (202) 628-8800 Fax No. (202) 628-8844					
				 SIGNATURE Vincent J. Sunderdick NAME 29,004 REGISTRATION NUMBER 11 September 2000 DATE	

00227 4622360

Attorney Docket: 951/49162  
PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: MARTIN PELLER ET AL.

Serial No.: NOT YET ASSIGNED PCT No.: PCT/EP99/01165

Filed: SEPTEMBER 11, 2000

Title: DATA BUS FOR A PLURALITY OF NODES

PRELIMINARY AMENDMENT

**Box PCT APPLICATION**

Commissioner for Patents  
Washington, D.C. 20231

Sir:

Please enter the following amendments to the specification, claims and abstract prior to the examination of the application.

IN THE SPECIFICATION:

A substitute specification is submitted herewith.

IN THE CLAIMS:

Please cancel claims 1 and 2 and add new claims 3-6 as follows:

-- 3. A data bus arrangement for a plurality of nodes connected to each other, said arrangement comprising:

a logical decision gate having a plurality of inputs corresponding to said plurality of nodes;

at least one converter module connected between said plurality of nodes and said logical decision gate, each convertor module converting an optical output from one of said nodes to an electrical signal which is fed to one of said inputs of said logical decision gate;

a plurality of switching means, each switching means connected between an output of said logical decision gate and an input of one of said convertor modules for controlling said convertor module independent of an output signal on the output of said decision gate.

4. The data bus arrangement according to Claim 3, wherein said switch means includes a control register addressable from a micro controller; and

an OR gate having a first input for receiving the output of said decision gate and the second input for receiving an output of said control register.

5. A method for controlling communication among a plurality of data nodes, comprising the steps of:

providing a decision gate having a plurality of inputs corresponding to said plurality of nodes;

providing at least one convertor module connected between said plurality of nodes and said logical decision gate, each

convertor module converting an optical out from one of said nodes to an electrical signal which is fed to one of said inputs of said logical decision gate;

outputting a signal from said logical decision gate to an input of each of said convertor modules;

providing a plurality of switchable control means, each of said plurality of switchable control means connected to one of said convertor modules for controlling said convertor module independent of an output signal on the output of said decision gate.--

**IN THE ABSTRACT:**

Please add an Abstract of the Disclosure submitted herewith on a separate page.

**REMARKS**

Entry of the amendments to the specification, claims and abstract, before examination of the application is respectfully requested.

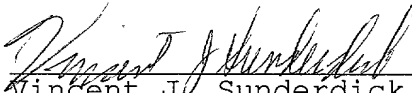
If there are any questions regarding this Preliminary Amendment or this application in general, a telephone call to the undersigned would be appreciated since this should expedite the prosecution of the application for all concerned.

It is respectfully requested that, if necessary to effect a timely response, this paper be considered as a Petition for an

Extension of Time sufficient to effect a timely response and shortages in other fees, be charged, or any overpayment in fees be credited, to the Account of Evenson, McKeown, Edwards & Lenahan, P.L.L.C., Deposit Account No. 05-1323 (Docket #951/49162).

Respectfully submitted,

September 11, 2000

  
\_\_\_\_\_  
Vincent J. Sunderdick  
Registration No. 29,004

VJS/rrt

EVENSON, McKEOWN, EDWARDS  
& LENAHA, P.L.L.C.  
1200 G Street, N.W., Suite 700  
Washington, DC 20005  
Telephone No.: (202) 628-8800  
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-- ABSTRACT OF THE DISCLOSURE

A data bus arrangement for a plurality of nodes connected to each other including a logical decision gate having a plurality of inputs corresponding to the number of nodes. A converter module is connected between each node and the logical decision gate. Each convertor module converts an optical output from one of the nodes to an electrical signal which is fed to one of the inputs of the logical decision gate. A separate switch is connected between an output of the logical decision gate and an input of each one of said convertor modules for controlling the convertor module independent of an output signal on the output of the decision gate.--

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(English Translation)  
WO 99/46894

1

PCT/EP99/01165

Data Bus for a Plurality of Nodes

The invention relates to a data bus for a plurality of nodes that are connected to one another via a star coupler. Such a data bus is known from the unpublished German patent application 19720401. Herein, the nodes are connected to the data bus via transmitter/sender modules as long as said nodes are operating properly. Said bus nodes are active even when they are not required. Depending on the type of application, however, deactivation of the entire data bus may not always be desired. After a vehicle is turned off, nodes serving the access control and antitheft protection systems should remain active even though all the rest of the nodes are not required.

The object of the invention is to provide a data bus of the aforementioned art that allows nodes to be selectively disconnected.

The object of the invention is achieved by the means of Claim 1.

This solution comprises a series of individual measures that in combination provide the desired effect. In one of such measures, optionally occurring optical signals in electrical form are converted and fed as input signals to the star coupler. Said star coupler itself comprises a logical decision gate to which input signals are fed, and whose output is connected to the inputs of the nodes in a parallel manner via an electrical line. A switch is arranged in parallel at least at the inputs of said nodes, which are disconnected when required. Said switch can optionally be activated, and interrupts the transmission segment between said decision gate and said node, thus disconnecting said node from the data bus.

An advantageous development of the invention is provided in Claim 2. Addressability of the switch enables only a single node to be disconnected from the data bus, if required, in a simple manner.

Finally, such a switch can be assigned to a group of nodes, which can always be connected or disconnected as a unit.

The invention is further illustrated by means of a single figure. Said figure shows a detail representation of a data bus according to the invention whereby the mode of

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transmission of the nodes is monitored.

At a data bus D are represented two nodes  $T_n$  and  $T_{n+1}$  that are connected via S/E (transmit/receive) modules  $S/E_n$  and  $S/E_{n+1}$ . Said  $S/E_n$  and  $S/E_{n+1}$  modules convert optical messages in electric form received from said  $T_n$  and  $T_{n+1}$  nodes and relay signals these  $Di_n$ ,  $Di_{n+1}$  as input signals to a logical decision gate (AND Gate 1) as the central component of a star coupler K. The number of inputs and outputs of said AND Gate 1 corresponds to the number of bus nodes. The output of said AND Gate 1 drives all inputs ( $Do_n$ ,  $Do_{n+1}$ ) of said  $S/E_n$  and  $S/E_{n+1}$  modules. Said modules convert these electrical signals into optical signals and transmit same to said  $T_n$  and  $T_{n+1}$  nodes via optical transmission segments, not shown.

A node can be disconnected from receiving bus communication. To this end, in each output path of the AND Gate 1 is provided an OR Gate 5 whose second input can be set to the high level via an output of a control register 6. Said control register 6 is addressable and is controlled by a serial interface (SPI, for example) of a microcontroller  $\mu C$ .

Thus, a low level can no longer proceed at the output of the AND Gate 1 to the input of the assigned  $S/E_n$  or  $S/E_{n+1}$  modules. The connected node cannot receive messages, and can remain in sleep mode, for example. With this function, nodes can be disconnected from the bus communication, either individually or in groups.

Should the node be reactivated, the control register 6 can be deactivated and the OR Gate 5 can once again be made conductive for a low level.

## Data Bus for a Plurality of Nodes

### Patent Claims

1. Data bus for a plurality of nodes that are connected to one another via a star coupler, characterized in that the input signals of said star coupler exist in electrical form, that said star coupler comprises a logical decision gate at whose inputs the outputs of said nodes are connected and to which the input signals are fed, that the output of said decision gate is connected to the inputs of said nodes in a parallel manner via an electrical line, that at least one part of said nodes is connected to optoelectric transducers via an optical transmission segment, said transducers being connected on the load side or on the line side and being situated on said star coupler, and that the inputs of said nodes are connected to the electrical line via a switch that can be controlled independently of the node.
2. Data bus according to Claim 1, characterized in that the switch is addressable.

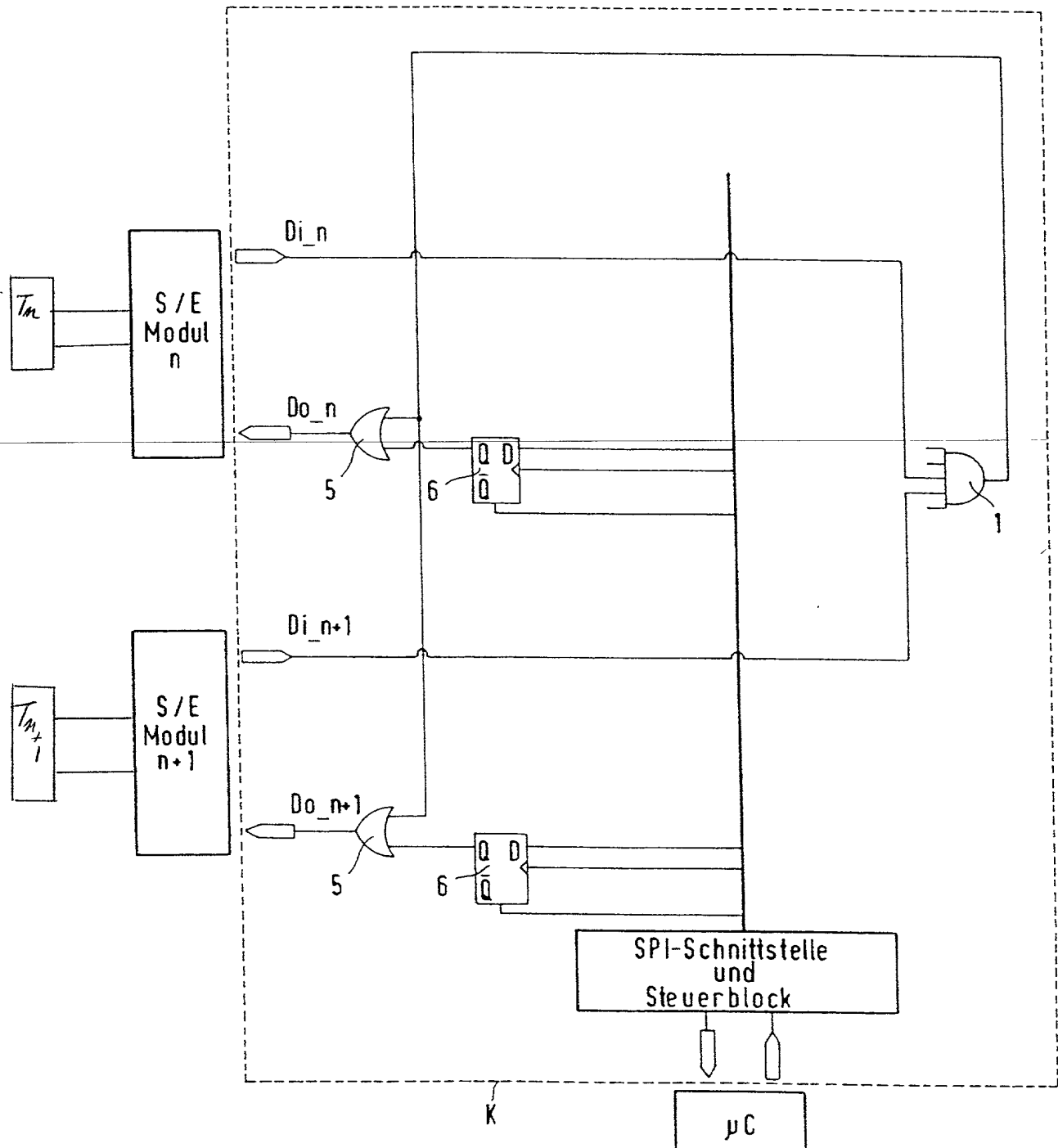
Key to Figure:

S/E Modul n = transmit/receive module n

S/E Modul n+1 = transmit/receive module n+1

SPI-Schnittstelle und  
Steuerblock = SPI interface and control block

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1/PART

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Clean Specification  
PCT/EP99/01165

TITLE OF THE INVENTION

**Data Bus for a Plurality of Nodes**

This application claims the priority of German Patent Application  
5 198 10 291.7, filed March 10, 1998 and PCT/EP99/01165 filed  
October 3, 1998, the disclosures of which are expressly  
incorporated by reference herein.

09/623894  
11/24/00  
The invention relates to a data bus for a plurality of nodes that  
are connected to one another via a star coupler. Such a data bus  
is known from the unpublished German patent application 19720401.  
Herein, the nodes are connected to the data bus via  
transmitter/sender modules as long as nodes are operating  
properly. bus nodes are active even when they are not required.  
Depending on the type of application, however, deactivation of  
15 the entire data bus may not always be desirable. After a vehicle  
is turned off, nodes serving the access control and antitheft  
protection systems should remain active even though all the rest  
of the nodes are not required.

20 The object of the invention is to provide a data bus of the  
aforementioned type that allows nodes to be selectively  
disconnected.

According to the present invention, a series of individual measures in combination provide the desired effect. In one of such measures, optionally occurring optical signals are converted to electrical signals and fed as input signals to the star coupler arrangement. The star coupler arrangement itself includes a logical decision gate to which input signals are fed, whose output is connected to the inputs of the nodes in a parallel manner via an electrical line. A switch is arranged in parallel at least at the inputs of the nodes, which are disconnected when required. The switch can optionally be activated, and interrupts the transmission segment between said decision gate and said node, thus disconnecting said node from the data bus.

In an advantageous development of the invention the addressability of the switch enables only a single node to be disconnected from the data bus, if required, in a simple manner.

Finally, such a switch can be assigned to a group of nodes, which can always be connected or disconnected as a unit.

Other objects, advantages and novel features of the present invention will become apparent from the following detailed

description of the invention when considered in conjunction with the accompanying drawings.

#### BRIEF DESCRIPTION OF THE DRAWINGS

The single figure shows a detail representation of a data bus according to the invention whereby the mode of transmission of the nodes is monitored.

#### DETAILED DESCRIPTION OF THE DRAWINGS

At a data bus  $D$  are represented two nodes  $T_n$  and  $T_{n+1}$  that are connected via S/E (transmit/receive) modules  $S/E_n$  and  $S/E_{n+1}$ . The  $S/E_n$  and  $S/E_{n+1}$  modules convert optical messages in electric form received from the  $T_n$  and  $T_{n+1}$  nodes and relay these signals  $Di_n$ ,  $Di_{n+1}$  as input signals to a logical decision gate (AND Gate 1) as the central component of a star coupler  $K$ . The number of inputs and outputs of AND Gate 1 corresponds to the number of bus nodes. The output of AND Gate 1 drives all inputs ( $Do_n$ ,  $Do_{n+1}$ ) of the  $S/E_n$  and  $S/E_{n+1}$  modules. The modules convert these electrical signals into optical signals and transmit same to  $T_n$  and  $T_{n+1}$  nodes via optical transmission segments.

A node can be disconnected from receiving bus communication. To this end, in each output path of the AND Gate 1 is provided an

OR Gate 5 whose second input can be set to the high level via an output of a control register 6. The control register 6 is addressable and is controlled by a serial interface (SPI, for example) of a microcontroller  $\mu C$ .

5 Thus, a low level can no longer proceed from the output of the AND Gate 1 to the input of the assigned  $S/E_n$  or  $S/E_{n+1}$  modules. The connected node cannot receive messages, and can remain in sleep mode, for example. With this function, nodes can be disconnected from the bus communication, either individually or  
10 in groups.

When the node is reactivated, the control register 6 can be deactivated and the OR Gate 5 can once again be made conductive for a low level.

The foregoing disclosure has been set forth merely to illustrate  
15 the invention and is not intended to be limiting. Since modifications of the disclosed embodiments incorporating the spirit and substance of the invention may occur to persons skilled in the art, the invention should be construed to include everything within the scope of the appended claims and  
20 equivalents thereof.



WHAT IS CLAIMED IS

1. Data bus for a plurality of nodes that are connected to one another via a star coupler, characterized in that the input signals of said star coupler exist in electrical form, that said star coupler comprises a logical decision gate at whose inputs the outputs of said nodes are connected and to which the input signals are fed, that the output of said decision gate is connected to the inputs of said nodes in a parallel manner via an electrical line, that at least one part of said nodes is connected to optoelectric transducers via an optical transmission segment, said transducers being connected on the load side or on the line side and being situated on said star coupler, and that the inputs of said nodes are connected to the electrical line via a switch that can be controlled independently of the node.
2. Data bus according to Claim 1, characterized in that the switch is addressable.

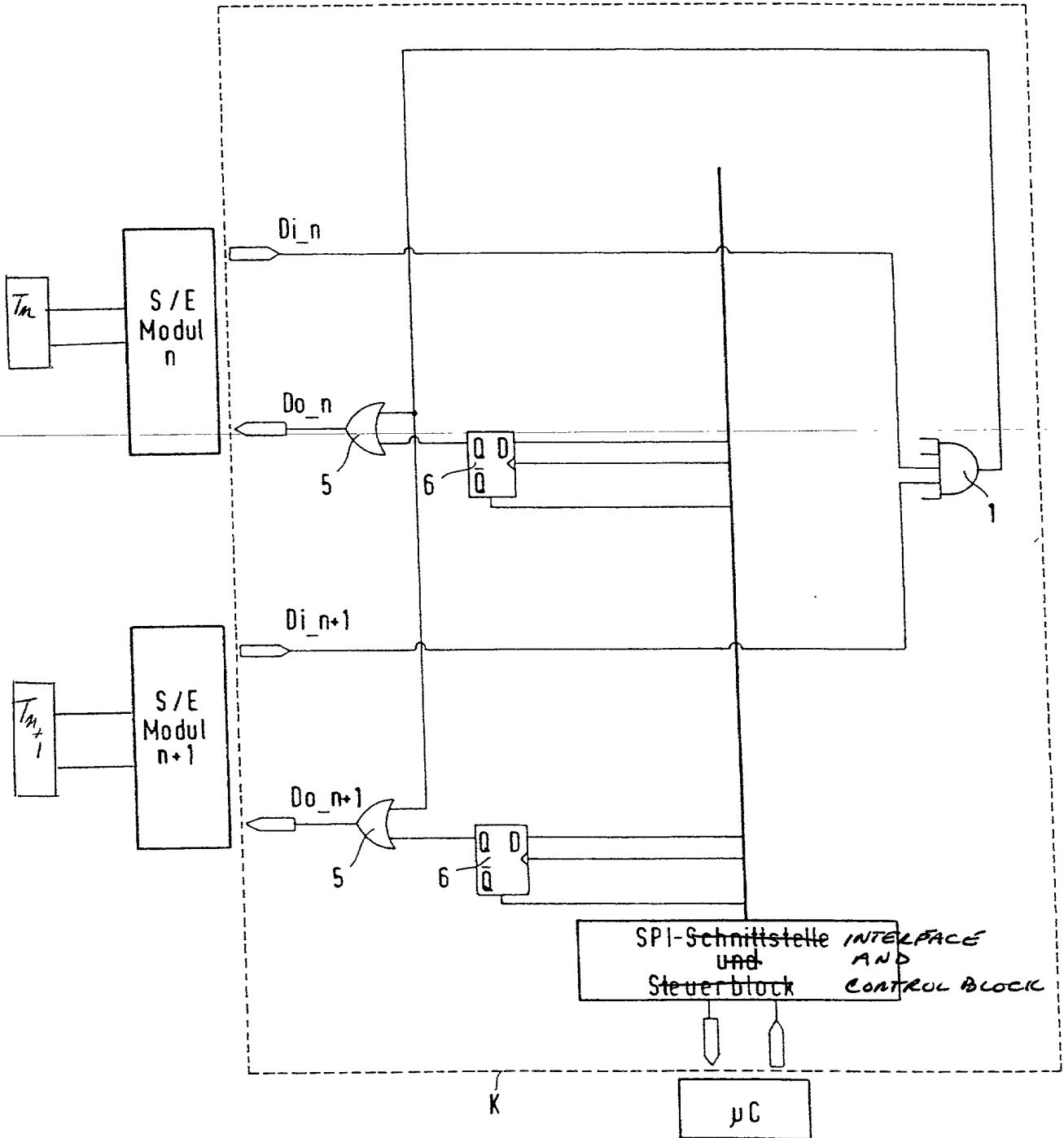
Key to Figure:

S/E Modul n = transmit/receive module n

S/E Modul n+1 = transmit/receive module n+1

SPI-Schnittstelle und

Steuerblock = SPI interface and control block



COMBINED DECLARATION FOR PATENT APPLICATION AND POWER OF ATTORNEY  
(includes Reference to PCT International Applications)

ATTORNEY'S DOCKET  
NUMBER

951/49162

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Data Bus For A Plurality of Nodes

the specification of which (check only one item below):

☐ is attached hereto.

☐ was filed as United States application

Serial No. \_\_\_\_\_

on \_\_\_\_\_

and was amended

on \_\_\_\_\_ (if applicable).

☒ was filed as PCT international application

Number PCT/EP99/01165

on October 3, 1998

and was amended under PCT Article 19

on \_\_\_\_\_ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations. §1.56(a).

I hereby claim foreign priority benefits under Title 35, United State Code, §119 of any foreign application(s) for patent or inventor's certificate or of any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed:

PRIOR FOREIGN/PCT APPLICATION(S) AND ANY PRIORITY CLAIMS UNDER 35 U.S.C. 119:

COUNTRY (if PCT indicate PCT)	APPLICATION NUMBER	DATE OF FILING (day, month, year)	PRIORITY CLAIMED UNDER 35 USC 119
Germany	198 10 291.7	10 March 1998	<input checked="" type="checkbox"/> Yes <input type="checkbox"/> No
			<input type="checkbox"/> Yes <input type="checkbox"/> No
			<input type="checkbox"/> Yes <input type="checkbox"/> No
			<input type="checkbox"/> Yes <input type="checkbox"/> No
			<input type="checkbox"/> Yes <input type="checkbox"/> No



23911

PATENT TRADEMARK OFFICE

Combined Declaration For Patent Application and Power of Attorney (Continued)  
(includes Reference to PCT international Applications)

ATTORNEY'S DOCKET NUMBER

951/49162

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) or PCT international application(s) designating the United States of America that is/are listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in that/those prior application(s) in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application(s) and the national of PCT international filing date of this application:

PRIOR U.S. APPLICATIONS OR PCT INTERNATIONAL APPLICATIONS DESIGNATING THE U.S. FOR BENEFIT  
UNDER 35 U.S.C. 120

U.S. APPLICATIONS

STATUS (Check one)

U.S. APPLICATION  
NUMBER

U.S. FILING DATE

PATENTED

PENDING

ABANDONED

PCT APPLICATIONS DESIGNATING THE U.S.

PCT APPLICATION  
NO

PCT FILING  
DATE

U.S. SERIAL NUMBERS ASSIGNED (IF  
ANY)

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. (List name and registration number)

Martin Fleit, Reg. No. 16,900; Herbert I. Cantor, Reg. No. 24,392; James F. McKeown, Reg. No. 25,406;  
Donald D. Evenson, Reg. No. 26,160; Joseph D. Evans, Reg. No. 26,269; Gary R. Edwards, Reg. No.  
31,824; Jeffrey D. Sanok, Reg. No. 32,169; and Richard R. Diefendorf, Reg. No. 32,390

Send Correspondence to:

Evenson, McKeown, Edwards & Lenahan, P.L.L.C.  
1200 G Street, N.W., Suite 700  
Washington, D.C. 20005

Direct Telephone Calls to:  
(name and telephone number)

(202) 628-8800

201	FULL NAME OF INVENTOR	FAMILY NAME	FIRST GIVEN NAME	SECOND GIVEN NAME
	RESIDENCE & CITIZENSHIP	CITY	STATE OR FOREIGN COUNTRY	COUNTRY OF CITIZENSHIP
	POST OFFICE ADDRESS	POST OFFICE ADDRESS	CITY	STATE & ZIP CODE/COUNTRY
202	FULL NAME OF INVENTOR	FAMILY NAME	FIRST GIVEN NAME	SECOND GIVEN NAME
	RESIDENCE & CITIZENSHIP	CITY	STATE OR FOREIGN COUNTRY	COUNTRY OF CITIZENSHIP
	POST OFFICE ADDRESS	POST OFFICE ADDRESS	CITY	STATE & ZIP CODE/COUNTRY
203	FULL NAME OF INVENTOR	FAMILY NAME	FIRST GIVEN NAME	SECOND GIVEN NAME
	RESIDENCE & CITIZENSHIP	CITY	STATE OR FOREIGN COUNTRY	COUNTRY OF CITIZENSHIP
	POST OFFICE ADDRESS	POST OFFICE ADDRESS	CITY	STATE & ZIP CODE/COUNTRY

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

SIGNATURE OF INVENTOR 201

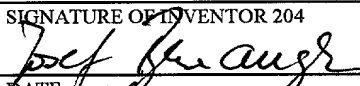
SIGNATURE OF INVENTOR 202

SIGNATURE OF INVENTOR 203

DATE

DATE

DATE

Combined Declaration For Patent Application and Power of Attorney (Continued) (includes Reference to PCT international Applications)				ATTORNEY'S DOCKET NUMBER  951/49162	
I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) or PCT international application(s) designating the United States of America that is/are listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in that/those prior application(s) in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application(s) and the national of PCT international filing date of this application:					
PRIOR U.S. APPLICATIONS OR PCT INTERNATIONAL APPLICATIONS DESIGNATING THE U.S. FOR BENEFIT UNDER 35 U.S.C. 120					
U.S. APPLICATIONS			STATUS (Check one)		
U.S. APPLICATION NUMBER	U.S. FILING DATE		PATENTED	PENDING	ABANDONED
PCT APPLICATIONS DESIGNATING THE U.S.					
PCT APPLICATION NO	PCT FILING DATE	U.S. SERIAL NUMBERS ASSIGNED (IF ANY)			
<p>POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. (List name and registration number)</p> <p style="text-align: center;">Herbert I. Cantor, Reg. No. 24,392; James F. McKeown, Reg. No. 25,406; Donald D. Evenson, Reg. No. 26,160; Joseph D. Evans, Reg. No. 26,269; Gary R. Edwards, Reg. No. 31,824; and Jeffrey D. Sanok, Reg. No. 32,169</p>					
Send Correspondence to:			Direct Telephone Calls to: (name and telephone number)		
Evenson, McKeown, Edwards & Lenahan, P.L.L.C. 1200 G Street, N.W., Suite 700 Washington, D.C. 20005			(202) 628-8800		
204	FULL NAME OF INVENTOR	FAMILY NAME <u>BERWANGER</u>	FIRST GIVEN NAME <u>Josef</u>		SECOND GIVEN NAME
	RESIDENCE & CITIZENSHIP	CITY <u>Poing</u>	STATE OR FOREIGN COUNTRY		COUNTRY OF CITIZENSHIP <u>Germany</u>
	POST OFFICE ADDRESS	POST OFFICE ADDRESS <u>Parkweg 1</u>	CITY <u>Poing</u>		STATE & ZIP CODE/COUNTRY <u>D-85586, Germany DEX</u>
205	FULL NAME OF INVENTOR	FAMILY NAME	FIRST GIVEN NAME		SECOND GIVEN NAME
	RESIDENCE & CITIZENSHIP	CITY	STATE OR FOREIGN COUNTRY		COUNTRY OF CITIZENSHIP
	POST OFFICE ADDRESS	POST OFFICE ADDRESS	CITY		STATE & ZIP CODE/COUNTRY
206	FULL NAME OF INVENTOR	FAMILY NAME	FIRST GIVEN NAME		SECOND GIVEN NAME
	RESIDENCE & CITIZENSHIP	CITY	STATE OR FOREIGN COUNTRY		COUNTRY OF CITIZENSHIP
	POST OFFICE ADDRESS	POST OFFICE ADDRESS	CITY		STATE & ZIP CODE/COUNTRY
I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.					
SIGNATURE OF INVENTOR 204 		SIGNATURE OF INVENTOR 205		SIGNATURE OF INVENTOR 206	
DATE <u>28.08.2005</u>		Date		DATE	